UNIVERSITY OF DERBY

School of Arts, Design and Technology

EXAMINATION PAPER

BSc/BSc (Hons) MUSIC TECHNOLOGY & AUDIO SYSTEMS DESIGN
BSc/BSc (Hons) SOUND, LIGHT AND LIVE EVENT TECHNOLOGY
BSc/BSc (Hons) ELECTRICAL AND ELECTRONIC ENGINEERING
LEVEL SIX

EMBEDDED SYSTEMS
6EJ005

DATE: **SUMMER 2004**

TIME ALLOWED: 2 HOURS

Instructions to Candidates

1. Answer all *three* questions
2. All questions carry equal marks

DO NOT TURN OVER UNTIL INSTRUCTED

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1. A simple hand-held device is being developed to assist in music education in schools. The device will hold a bank of simple tunes, which it can play back, and which can be selected by the teacher. The device is to be based around a PIC 16F84, as shown in Fig. Q1.1. The device has the further characteristics listed below.

   User Interface.
   a) Control will take the form of a set of 4 push button switches. The sequence in which the teacher presses these, within a certain time frame, determines the tune selected.
   b) One led is required to indicate power is applied. The led used has a forward voltage when in conduction of 1.8V, and requires around 5mA for adequate illumination.

   Music Output. This will be via a MAX538 serial Digital to Analogue Converter (DAC), as detailed in Fig Q1.2. Its analogue output will drive a low-power amplifier module, which in turn will drive a small loudspeaker.

Develop a preliminary design for this device including the following:
i) Any calculations made.
ii) Any assumptions made, with explanations.
iii) A complete circuit diagram, including microcontroller and DAC, all interconnections, proposed power source, and all other components and their values (where possible). The amplifier module and loudspeaker can be shown as blocks, and the reference voltage for the DAC can be omitted.
iv) Noting that the 16F84 does not contain a serial port, explain briefly how the requirements of the serial interface can be met.

100%

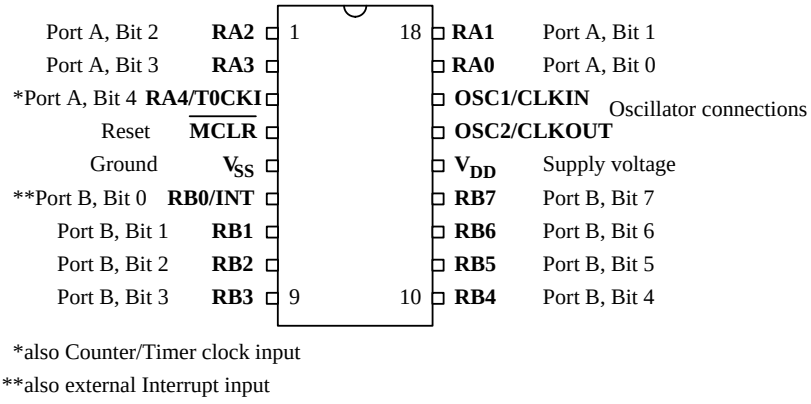
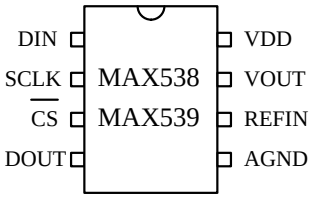


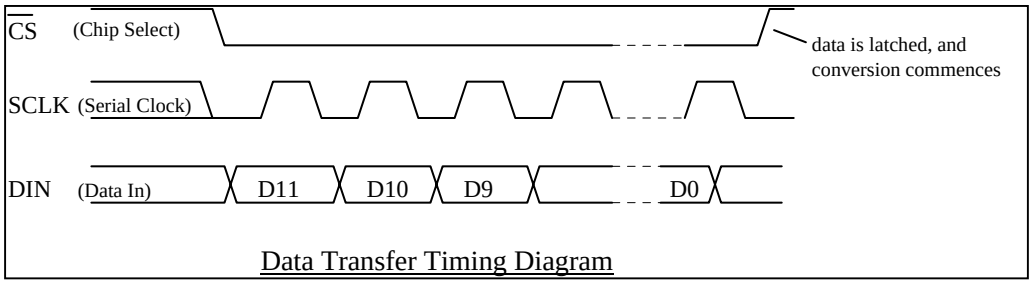
Fig Q1.1: PIC 16F84 Pinout



DIN: Data Input
SCLK: Serial Clock
CS: Chip Select
DOUT: Data Output
VDD: Supply Voltage
VOUT: Analogue Output Voltage
REFIN: Reference Voltage Input
AGND: Analogue Ground

Family Highlights

* Integrates the R-2R ladder with serial interface, op amp output, and voltage reference, in one easy-to-use sub-system
* Single supply, 4.5V to 5.5V
* Buffered voltage output
* Low supply current: (140uA MAX538/539)



Data Transfer Timing Diagram

Fig Q 1.2: MAX 538/9 Digital to Analogue Converter

2. i)A machine counts envelopes which are being packaged in packs of 150. The machine is controlled by a PIC 16F84. A sensor connected to the RA4/T0CK1 pin produces a logic pulse every time an envelope passes it. A block diagram of the Timer 0 module is shown in Fig. Q2.1, and the Option register in Fig Q 2.2.

a) Describe how you would configure the TMR0 to count the envelopes. Indicate what value you would set in the Option register.
b) Explain what strategy could be used to allow the microcontroller programme to detect when the number 150 had been reached.

60%

ii) In another application also using the 16F84, a regular timed interrupt is required. The clock oscillator frequency is 4MHz, and an interrupt frequency in the region of every 2ms is required. Describe how you would now configure the TMR0 module.

40%

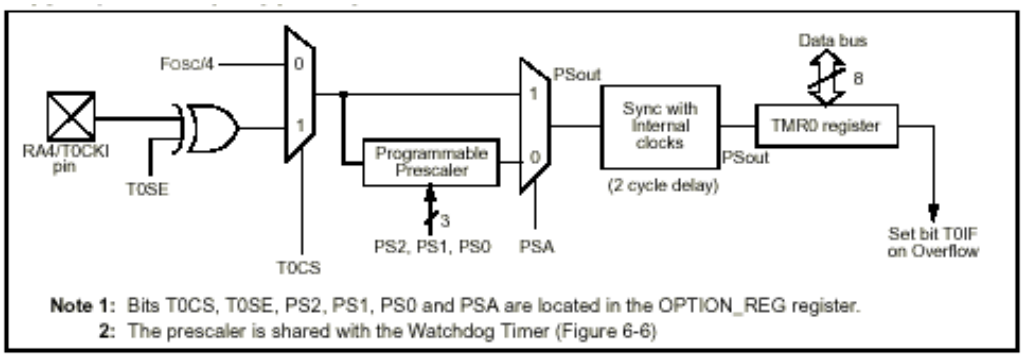


Fig. Q 2.1: The 16F84 TMR0 Module

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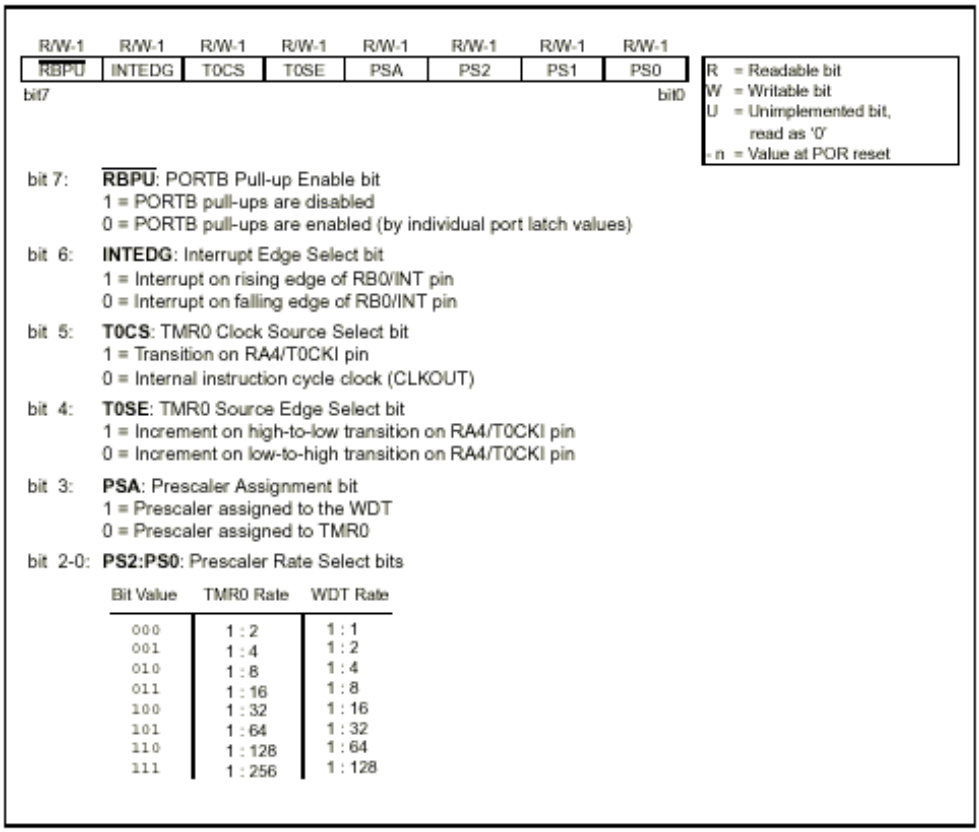


Fig. Q 2.2: The 16F84 Option Register

3. i) The interrupt logic of the PIC 16F84, typical of a simple microcontroller, is shown in Fig. Q3.1. The interrupt logic of the 80C552, typical of a medium complexity microcontroller, is shown in Fig Q3.2.

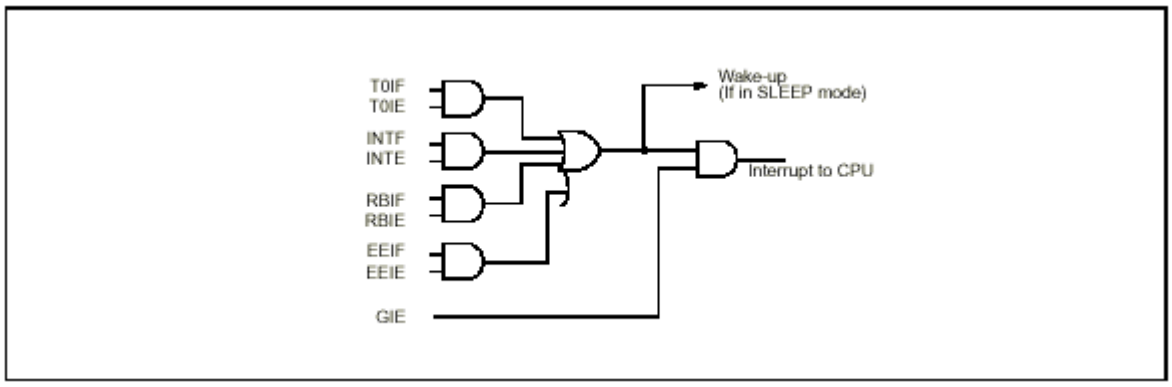
Describe the key differences and similarities between these two structures. What are the limitations of the 16F84 structure, and how is this overcome, if at all, in the 80C552? What are the limitations of the 80C552 structure, if any? **60%**

ii) A certain microcontroller programme has the following features:

Interrupt 1: highest priority, always enabled. Interrupt Service Routine (ISR) duration of 2ms.
Interrupt 2: disabled during critical region below. ISR duration of 500μs.
Critical region: Duration 12ms.

The longest instruction execution time of the microcontroller is 8μs, and its response time once the interrupt has been recognised is 4μs.

What is the worst-case interrupt latency for *each* interrupt? **40%**



Interrupt Vector Address: 0004 (Hex)

Fig. Q 3.1: The 16F84 Interrupt Logic, with Vector Address

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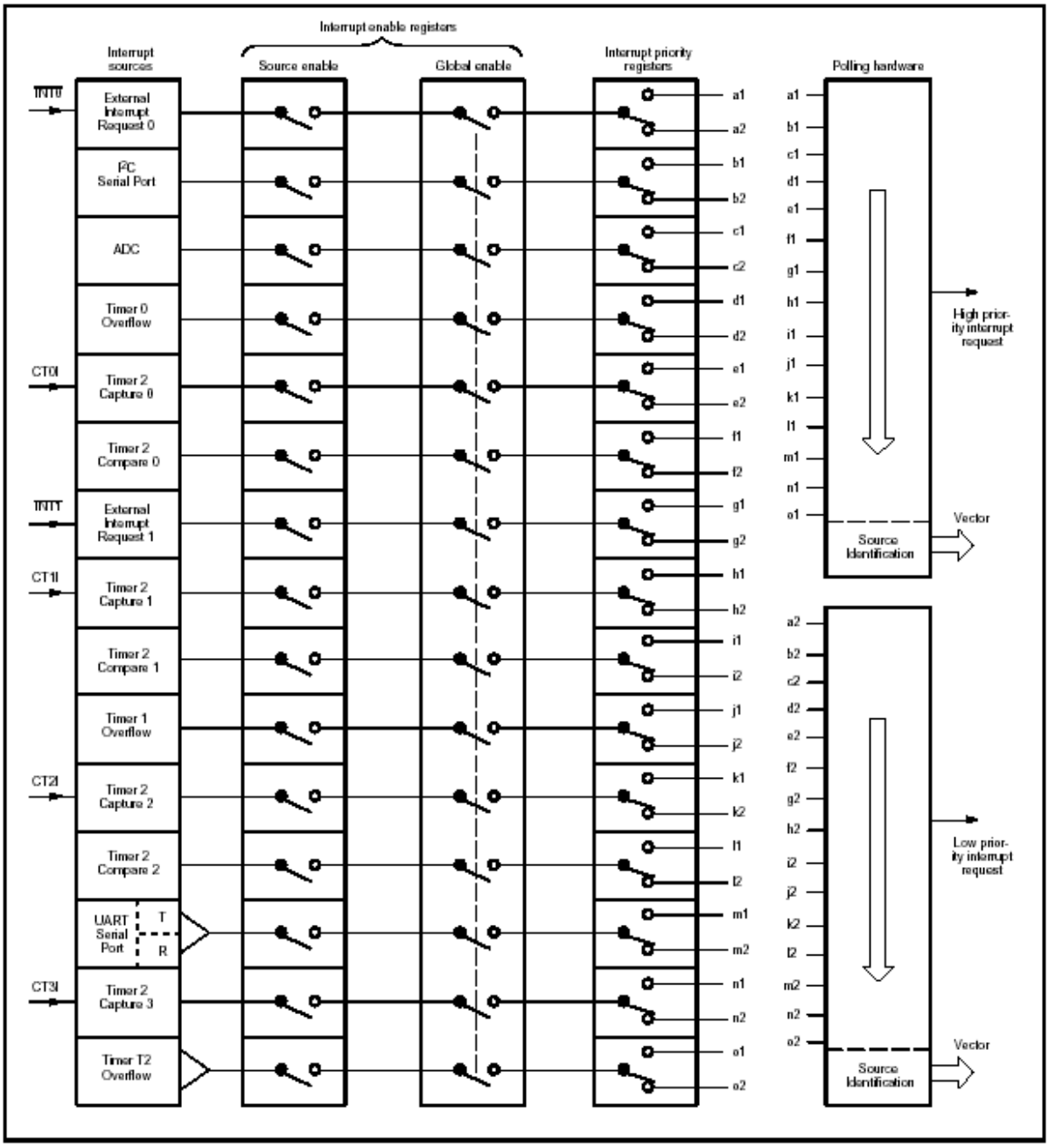
Interrupt enable registers
Interrupt sources
Source enable
Global enable
Interrupt priority registers
Polling hardware
INT0
External Interrupt Request 0
I²C Serial Port
ADC
Timer 0 Overflow
CT0I
Timer 2 Capture 0
Timer 2 Compare 0
INT1
External Interrupt Request 1
CT1I
Timer 2 Capture 1
Timer 2 Compare 1
Timer 1 Overflow
CT2I
Timer 2 Capture 2
Timer 2 Compare 2
UART Serial Port
T
R
CT3I
Timer 2 Capture 3
Timer T2 Overflow
a1 a2 b1 b2 c1 c2 d1 d2 e1 e2 f1 f2 g1 g2 h1 h2 i1 i2 j1 j2 k1 k2 l1 l2 m1 m2 n1 n2 o1 o2
High priority interrupt request
Low priority interrupt request
Vector
Source Identification

TURN OVER

SOURCE	NAME	VECTOR ADDRESS
External interrupt 0	X0	0003H
Timer 0 overflow	T0	000BH
External interrupt 1	X1	0013H
Timer 1 overflow	T1	001BH
SIO0 (UART)	S0	0023H
SIO1 (I^2C)	S1	002BH
T2 capture 0	CT0	0033H
T2 capture 1	CT1	003BH
T2 capture 2	CT2	0043H
T2 capture 3	CT3	004BH
ADC completion	ADC	0053H
T2 compare 0	CM0	005BH
T2 compare 1	CM1	0063H
T2 compare 2	CM2	006BH
T2 overflow	T2	0073H

Fig. Q 3.2: The 80C552 Interrupt Logic, with Vector Addresses